Confidential Computing

UK RISE Annual Conference 2020



Computing Platforms & Problem Statement

- Compromise of confidentiality
 - code and data are exposed in plain text on computing platforms
 - when "in use"
 - compromise of user data leading to the loss of privacy
 - from constrained IoT devices to cloud deployments
- Compromise of code and data integrity

- How to ensure that computing platforms are trustworthy and correct software is run on them?
- Making HW Root of Trust (RoT) available to guests in cloud deployments is challenging
- Compromise of IPR
 - e.g. algorithms, ML models,..

What does Confidential Computing mean?

- Code and data confidentiality can be achieved at runtime ("in use")
 - e.g. by means of **HW based isolation** and **memory/CPU state encryption technologies**
- Data confidentiality and integrity can be protected at rest, in use and in transit
- Code and data cannot be tampered and accessed from outside of the trust boundaries of a secure enclave/trust domain
- Code and data can be **measured** and **attested**.
 - Confidential Computing is built upon the existing concepts of Trusted Computing

... and the relevant technologies allow all of these to be achieved both on **bare metal** and in **virtualized environments**

The relevant technologies



Intel MKTME (Multi Key Total Memory Encryption) Intel TDX (Trust Domain Extensions) Intel SGX (Software Guard Extensions) <u>AMD SEV</u> (Secure Encrypted Virtualization) <u>AMD SEV-SNP</u> (Secure Encrypted Virtualization – Secure Nested Paging)

The use cases



The relevant open source projects

• Intel SGX SDK

- provided by Intel for developing Intel SGX secure enclaves
- provides libraries, headers, samples codes, tools and documentation

Open Enclave SDK

• open source SDK that mostly hides underlying enclave technology and initiated by Microsoft

<u>Google Asylo</u>

- open source SDK that mostly hides underlying enclave technology and initiated by Google
- <u>Google Project Oak</u>: Control and end to end encryption of data in distributed systems

• <u>Apache Teaclave</u>

- <u>Crypto API Toolkit</u> (Intel SGX based softHSM)
- Baidu Rust SGX SDK
- Fortanix Rust SGX SDK
- Enarx
- <u>RISC-V Keystone</u>
- <u>RISC-V HexFive</u>
- <u>Hyperledger Private Data Objects</u> (Blockchain by Intel)
- <u>The Confidential Consortium (CoCo) Framework</u> (Blockchain by Microsoft)
- <u>Hyperledger Fabric Private Chaincode</u> (Blockchain by IBM)

What else is happening?

- <u>The Confidential Computing Consortium</u>
 - <u>Announced on August 21st, 2019 by the</u> <u>Linux Foundation</u>
 - An industry wide effort
 - to advance computational trust and security for next-generation computing
 - to bring together HW and SW vendors, cloud providers, developers, open source experts and academics to accelerate the confidential computing market
 - to influence the relevant technical and regulatory standards

- Growing number startup companies emerging and providing services/products related to Confidential Computing
- Commercial availability of "Confidential Computing" capabilities by the cloud vendors
- Lots of academic research on
 - finding novel solutions utilizing Confidential Computing Technologies
 - microarchitectural side channel attacks and mitigations
 - some interesting projects such as <u>Slalom</u>, <u>Project Graviton</u> and <u>CoSMIX</u>

The solutions for encrypting applications, containers and VMs

OCI encrypted container images	Enarx	Intel SGX Protected Code Launch (PCL)	VMware vSphere VM encryption
 Allows encryption container later 	 An application deployment framework 	 <u>PCL</u> allows running encrypted code and data 	 <u>VMware vSphere VM</u> <u>encryption</u> allows encryption of VM
 Encryption can be done by using <u>Containerd imgcrypt</u> 	 Support both AMD SEV an Intel SGX. Intel TDX to follow 	 "<u>sgx_encrypt</u>" tool encrypts the sections of a secure enclave 	images and VM disk images
 <u>library</u> or <u>skopeo tool</u> Also see <u>OClcrypt</u> and 	 In case of AMD SEV, Enarx allows 	(except .bss, .tbss, .dynamic, .debug,) by using AES GCM	 Integration with vCenter Server and KMS
the specification proposal. The work also includes <u>Kubernetes integration</u>	Cificationdeployment ofI. The workencrypted workloadsludesto AMD SEV afteretes integrationattestation and keyprovisioning processes	 Content key is provisioned y using a sealing enclave IP enclave by using sgx create encrypt 	

ed enclave()

What about Homomorphic Encryption?

- Homomorphic Encryption (HE) refers to an encryption scheme "<u>that allows computation to be</u> <u>directly on encrypted data, without requiring any decryption in the process</u>"
- Invented in 2009
 - but the origins go back to a paper (titled as "<u>On Data Banks and Privacy</u> <u>Homomorphisms</u>") published by Ronald Linn Rivest and Len Adleman in 1978
 - (Ronald L. Rivest invented RSA algorithm together with Adi Shamir and Len Adleman in 1977)
 - the existence of a Full HE scheme was demonstrated in 2009 by Craig Gentry
- Publicly available SW implementations are available: <u>Microsoft SEAL</u>, <u>HELib</u> (IBM) and <u>PALISADE</u>
- FHE is far from being practical due to massive overhead in computation and memory

Attestation is a process of measuring code and data; and reporting these measurements as digitally signed to a requesting entity, which can evaluate these measurements further according to known values or whitelists.

What is needed for a fully functional attestation mechanism ?

HW RoT	Attester	Protocol	Verifier	Relying Party
HW RoT for storage, reporting and measurement Crypto functionality	SW APIs for accessing crypto modules/the secure enclaves functionality	An attestation protocol between attestor and verifier	Being able to validate, verify and evaluate attestation reports	Relies on attestation verification results provided by the Verifier
Cryptographic identities for attestation	Attestation agent and the relevant services	scalable protocol that can mitigate known attacks (e.g. replay attacks)	capabilities for updating whitelists, etc. Keeping whitelists up to date	Applies specific actions based on attestation results

IETF RATS (Remote ATtestation procedureS) architectural overview

Appraisal Policy for Evidence	Appraisal Policy for Evidence: A set of rules that informs how a Verifier evaluates the validity of information about an Attester	End	orser		Refer Val Ow	rence ue mer		Verifier Owner		Relying Ow	j Party ner
Attester	An entity providing evidence that must be appraised in order to infer the extent to which the Attester is considered trustworthy			Ref v	erence alues			Apprai: for e	sal polic vidence	ÿ	
Endorser	An entity (typically a manufacturer) whose Endorsements help Verifiers appraise the authenticity of Evidence	Endorsements		\downarrow		Ap at	Appraisal policy for attestation results				
Evidence	A set of information (digitally signed) about an Attester that is to be appraised by a Verifier		\square		→	Ve	rifier				
Relying Party	A role performed by an entity that depends on the validity of information about an Attester, for purposes of reliably applying application specific actions	Evidence		_				Attestation results			
Relying Party Owner	An entity (typically an administrator), that is authorized to configure Appraisal Policy for Attestation Results in a Relying Party			1						_↓,	/
Verifier	A role performed by an entity that appraises the validity of Evidence about an Attester and produces Attestation Results to be used by a Relying Party	Atte	ester							Relying	g Party

Intel SGX DCAP overview



Intel SGX DCAP attestation data

• Attestation report body includes the following information (see sgx report body t)

typedef struct _report_body_t

sgx_cpu_svn_t	<pre>cpu_svn; /* (0) Security Version of the CPU */</pre>
<pre>sgx_misc_select_t</pre>	<pre>misc_select; /* (16) Which fields defined in SSA.MISC */</pre>
uint8_t	<pre>reserved1[SGX_REPORT_BODY_RESERVED1_BYTES]; /* (20) */</pre>
<pre>sgx_isvext_prod_id_t</pre>	<pre>isv_ext_prod_id;/* (32) ISV assigned Extended Product ID */</pre>
<pre>sgx_attributes_t</pre>	attributes; /* (48) Any special Capabilities the Enclave possess */
<pre>sgx_measurement_t</pre>	<pre>mr_enclave;</pre>
uint8_t	<pre>reserved2[SGX_REPORT_BODY_RESERVED2_BYTES]; /* (96) */</pre>
<pre>sgx_measurement_t</pre>	<pre>mr_signer;</pre>
uint8_t	<pre>reserved3[SGX_REPORT_BODY_RESERVED3_BYTES]; /* (160) */</pre>
<pre>sgx_config_id_t</pre>	<pre>config_id; /* (192) CONFIGID */</pre>
sgx_prod_id_t	<pre>isv_prod_id; /* (256) Product ID of the Enclave */</pre>
sgx_isv_svn_t	<pre>isv_svn; /* (258) Security Version of the Enclave */</pre>
<pre>sgx_config_svn_t</pre>	config_svn; /* (260) CONFIGSVN */
uint8_t	<pre>reserved4[SGX_REPORT_BODY_RESERVED4_BYTES]; /* (262) */</pre>
<pre>sgx_isvfamily_id_t</pre>	<pre>isv_family_id; /* (304) ISV assigned Family ID */</pre>
<pre>sgx_report_data_t</pre>	<pre>report_data; /* (320) Data provided by the user */</pre>

} sgx_report_body_t;

• Intel SGX DCAP attestation quote. (see <u>sgx quote3 t</u>)

typedef struct _sgx_quote3_t {
 sgx_quote_header_t header;
 sgx_report_body_t report_body;
 uint32_t signature_data_len;
#ifdef _MSC_VER
#pragma warning(push)
#pragma warning (disable:4200)
#endif
 uint8_t signature_data[];
#ifdef _MSC_VER
#pragma warning(pop)
#endif
} sgx quote3 t;

Demo: PyTorch running in a secure enclave with encrypted input and output files



Graphene-SGX: https://github.com/oscarlab/graphene/

https://arxiv.org/pdf/2009.04390.pdf



https://www.ericsson.com/en/security

Are the secure enclave technologies secure?

There is no binary "yes/no" answer to this question and the answer depends on:

Adversaries and their capabilities	Deployments	HW & SW security vulnerabilities	Supply chain security
 adversaries with the advanced technical capabilities such as being able to initiate powerful attacks 	 with or without physical access to devices? secure key generation and provisioning? 	 security vulnerabilities? are the known vulnerabilities patched? 	 both HW and SW supply chain security well established vulnerability and incident management processes?

Timeline of the microarchitectural side channel vulnerabilities



L1DES	L1D Eviction Sampling
MFBDS	Microarchitectural Fill Buffer Data Sampling
MDSUM	Microarchitectural Data Sampling Uncacheable Memory
VRS	Vector Register Sampling

LVI Load Value Injection

MLPDS Microarchitectural Load Port Data Sampling

- RIDL Rogue In-flight Data Load
- TSX Transactional Synchronization Extensions

Ilhan Gurel | 2020-11-30 | Open | Page 19 of 19