SCARV: a side-channel hardened RISC-V platform

https://www.scarv.org https://github.com/scarv

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THALES

- Recap:

$$\begin{array}{lcllll}
\text{SCARV} & \simeq & \text{RISC-V} & + & \text{cryptography} & \\
 & \simeq & \text{RISC-V} & + & \text{cryptographic engineering} & \\
 & \simeq & \text{RISC-V} & + & \text{implementation} & + \ \text{implementation attacks}
\end{array}$$

where

$$\begin{array}{lcl}
\text{WP-A} & \simeq & \text{a side-channel resistant RISC-V implementation} \\
\text{WP-B} & \simeq & \text{RISC-V support for next-generation cryptography} \\
\text{WP-C} & \simeq & \text{a democratised side-channel evaluation lab.}
\end{array}$$

- Generic activities:

  1. **publications**:
     - “*Towards Micro-Architectural Leakage Simulators: Reverse Engineering Micro-Architectural Leakage Features is Practical*” [10] (EUROCRYPT’22).
     - “*HYDRA: a multi-core RISC-V with cryptographically useful modes of operation*” [14] (CARRV’22).
     - “*RISC-V Instruction Set Extensions for Lightweight Symmetric Cryptography*” [5, 6] (NIST LWC workshop, TCHES’23.1).
  2. **events**:
     - “*MIRACLE: MIcRo-ArChitectural Leakage Evaluation*” [13] (TCHES’22.1): best paper award.
     - *Constructive Side-Channel Analysis and Secure Design (COSADE’22)*: invited talk.
     - *Smart Card Research and Advanced Application Conference (CARDIS’22)*: invited talk.
     - *Topics in hArdware SEcurity and RISC-V (TASER’22)* workshop (Sept.’22; $\sim$ 160 registrations, $>$ 100 participants).

https://ches.iacr.org/2022/taser

- Specific activities: ISEs for NIST LWC candidates.

Definition

NIST define [15, Section 1]

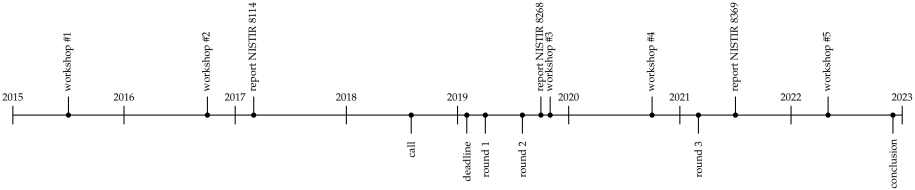
$$\text{lightweight cryptography} \;\simeq\; \text{“tailored for resource-constrained devices”}$$

e.g.,

- efficient on constrained hard/software platforms (vs. existing standards),
- efficient for short messages,
- amenable to countermeasures against implementation attacks,
- ...

with “efficient” read as low-latency, low-footprint, low-power, etc.

- Specific activities: ISEs for NIST LWC candidates.



  - 57 submissions,
  - 56 selected as round 1 candidates,
  - 32 selected as round 2 candidates,
  - 10 selected as round 3 candidates, i.e., finalists:

Name	Specification	AEAD	Hash	Component(s)
Grain128-AEAD	[12]	✓		Stream cipher
GIFT-COFB	[1]	✓		Block cipher
Romulus	[11]	✓	✓	(Tweakable) Block cipher
Ascon	[8]	✓	✓	Permutation
Elephant	[4]	✓		Permutation
PHOTON-Beetle	[2]	✓	✓	Permutation
Schwaemm and Esch	[3]	✓	✓	Permutation
Xoodyak	[7]	✓	✓	Permutation
ISAP	[9]	✓		Permutation
TinyJAMBU	[16]	✓		(Keyed) Permutation

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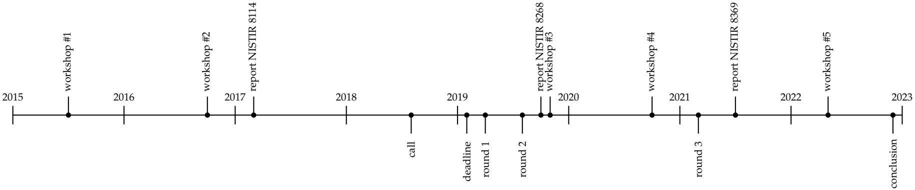

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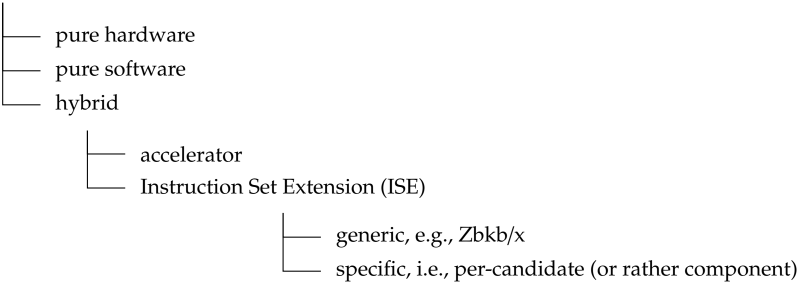
Name	Specification	AEAD	Hash	Component(s)
Grain128-AEAD	[12]	✓		L/NFSRs
GIFT-COFB	[1]	✓		GIFT-128
Romulus	[11]	✓	✓	Skinny-128-384+
Ascon	[8]	✓	✓	Ascon-p
Elephant	[4]	✓		Spongent-$\pi[n]$ or Keccak-$f[m]$
PHOTON-Beetle	[2]	✓	✓	$\texttt{PHOTON}_{256}$
Schwaemm and Esch	[3]	✓	✓	Sparkle (inc. Alzette ARX-box)
Xoodyak	[7]	✓	✓	Xoodoo
ISAP	[9]	✓		Ascon-p or Keccak-$f[m]$
TinyJAMBU	[16]	✓		P_n (inc. LFSR)

- Specific activities: ISEs for NIST LWC candidates.
  - options:



- pure hardware
- pure software
- hybrid
  - accelerator
  - Instruction Set Extension (ISE)
    - generic, e.g., Zbkb/x
    - specific, i.e., per-candidate (or rather component)

  - scope:
    - consider RV32 *and* RV64; focus on Rocket-based hardware
    - ignore hash API
    - ignore implementation attacks, bar data-independent latency
    - use “partial” component (e.g., only encryption) where possible
  - criteria:
    - strictly 3-address (i.e., 2-input, 1-output) instructions
    - disallow additional state (e.g., CSRs)

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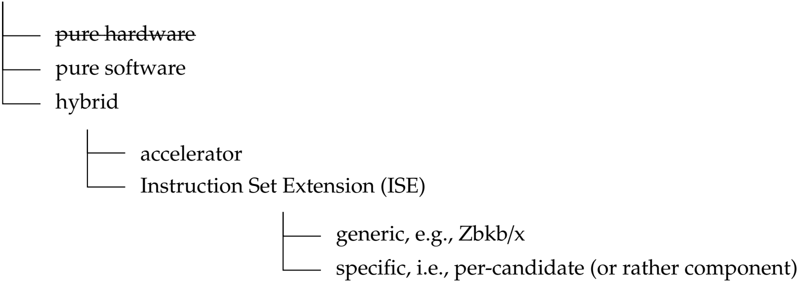

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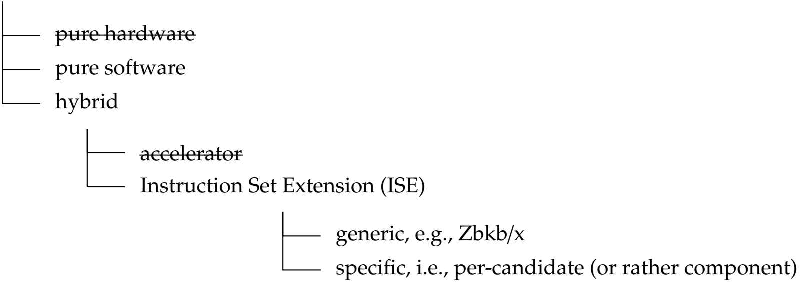

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Instruction Set Extension (ISE)

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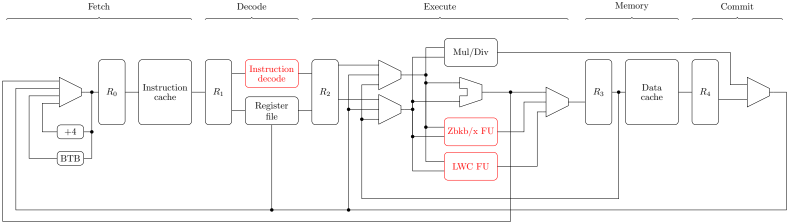
- Specific activities: ISEs for NIST LWC candidates.
  - strategy: for each candidate
    - analysis, then on-paper ISE design
    - software implementation using stock GCC-based tool-chain plus `.insn`
    - simulate using (patched) Spike
    - hardware implementation using Rocket



  - results (see [5, 6] for detail):
    - ISEs reduce software latency + footprint, at cost of some hardware overhead
    - ISEs reduce "gap" between hardware- and software-oriented candidates
    - Zbkb/x already makes significant impact
    - only ISE-assisted Schwaemm improves on ISE-assisted AES-GCM re. latency
    - ...

https://github.com/scarv/lwise

Questions?

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